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SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

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 APPLICANT
Hideto HIDAKA

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2818

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code: (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
cy		US 6,414,889	07/2002	Chen et al.	
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EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes - Number - Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No

OTHER ART (including Author, Title, Date, Patent, Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
cy		"A Precise On-Chip Voltage Generator for a Gigascale DRAM with a Negative Word-Line Scheme", by Tanaka et al., IEEE Journal of Solid-State Circuits, Vol. 34, No. 8, 8/1999, pp. 1084-1090.
cy		"Ultra LSI Memory" by Kiyoo Ito, Advanced Electronics Series, November 5, 1994, published by Baifukan, pp. 351-371.
cy		"An Experimental 256-Mb DRAM with Boosted Sense-Ground Scheme", by Asakura et al., IEEE Journal of Solid-State Circuits, Vol. 29, No. 11, 11/1994, pp. 1303-1309.

EXAMINER

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